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EXAMINER	
JOHNSTON, PHILLIP A	
ART UNIT	**PAPER NUMBER**
2881	

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/889,460	YON ET AL.	
	Examiner	**Art Unit**	
	Phillip A Johnston	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This Office Action is submitted in response to Amendment dated 3-18-2004, wherein Claims 17-32 are pending.

Claims Rejection – 35 U.S.C. 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 17-32, stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,021,663, to Hornbeck.

Hornbeck (663)clearly discloses in FIG. 3 a single bolometer, generally denoted by reference numeral 140, from array 106. The operation of array 106 is as follows: The chopped scene including warm body 116 is imaged onto array 106 which causes each R_B to fluctuate in value (with magnitude proportional to the temperature of the corresponding portion of the scene); the fluctuating value of R_B yields an alternating voltage across load resistor 143 which is fed to buffer amplifier 120 through capacitor 122. The outputs of buffer amplifiers 120 are read in column read out circuit 128 with a row at a time selected by row addressing circuit 130, which turns on pass transistors

132 in one row at a time (implies at least two detectors linked together, as recited in Claims 17 and 21).

FIGS. 4a-b are schematic cross sectional elevation views of bolometer 140 and FIG. 5a is a plan view; FIG. 5b illustrates in plan view a portion of array 106 showing the arrangement of the individual bolometers. Bolometer 140 includes a 1,700 ° thick and 50 microns square stack 144 made of a top 500° layer of silicon dioxide (oxide) 146, a 100 ° layer of titanium nitride (TiN) 148, a 500° layer of hydrogenated amorphous silicon (a-Si:H) 150 doped with boron to a carrier concentration of $2x10^{18}/cm^3$, another 100 ° layer of TiN 152, and a bottom 500 ° layer of silicon oxide 154. Stack 144 is supported over substrate 142 by two titanium tungsten (Ti:W) interconnects 156 and 158 located at diagonally opposite corners of the stack 144. As shown in FIG. 5a,stack 144 is square with two pairs of elongated openings 160, 162 and 164, 166 defining leads 170 and 174 between interconnects 156 and 158 and the remainder of stack 144 (resistor 141). Leads 170 and 174 are about 22 microns long and about 1.5 microns wide; this provides high thermal resistance. However, the heat loss from the main portion of stack 144 through leads 170 and 174 is more than an order of magnitude larger than the black-body radiation heat loss due to the temperature differential between resistor 141 and substrate 142. Upper electrode gap 172 separates upper oxide layer 146 and upper TiN layer 148 into two portions: one portion connected to interconnect 156 at contact 176 and the other portion connected to interconnect 158 at contact 178.

To maximize the signal voltage amplitude (which is the responsivity multiplied by the incident power), bolometer 140 should have a minimum thermal capacitance C and thermal conductance K and maximum active resistor absorbing area A, temperature coefficient α , and absorption ϵ. Bolometer 140 approaches these goals as follows. The thermal capacitance C is minimized by making stack 144 of thin films and the thermal conductance K is minimized by making leads 170 and 174 long and narrow. The active area A is maximized by integrating array 106 on a single silicon substrate and locating the detection circuitry under resistor 141 to provide high fill factor in array 106. See Column 3, line 20-61; and Column 7, line 31-43.

Hornbeck (663) also discloses in FIGS. 4a-b, oxide layer 190 covers and isolates load resistor R_L and buffer amplifier 120 and the remainder of silicon substrate 142 from aluminum ground plane 192. The distance from aluminum ground plane 192 to the bottom of stack 144 is about 2.5 microns for detection in the 8-12 micron wavelength range; this distance from ground plane 192 to stack 144 is one quarter wavelength for the range's center frequency. FIG. 4a schematically shows ground plane 192 as flat; whereas, FIG. 4b illustrates some of the underlying circuitry (CMOS) in substrate 142 and indicates the slight (few hundred °) unevenness of ground plane 192. TiN layers 148 and 152 provide the absorption of incident infrared radiation from the scene with warm body 116; amorphous silicon is transparent to infrared radiation. The quarter wavelength distance from ground plane 192 to stack 144 creates a quarter wavelength absorption filter for free carrier absorption in the thin, semi-transparent TiN 148 and 152 with an underlying quarter wavelength vacuum gap and ground plane

reflector. The uneveness of ground plane 192 has minimal effect on the absorption. Note that use of a vacuum gap for the absorption filter limits the thermal capacitance of stack 144 as compared to the use of a dielectric in the gap. See Column 8, line 32-56.

Hornbeck (663) further discloses further preferred embodiment bolometers and arrays are illustrated in plan views in FIGS. 9a-e; these plan views are analogs of FIG. 5a for bolometer 140 and show the suspended resistor, leads, and interconnect to the underlying substrate containing the load resistor, signal voltage amplifier, and addressing. In particular, the upper electrode gap analogous to gap 172 of bolometer 140 is indicated by a broken line 272 in each FIGS. 9a-e, and the interconnects to the substrate analogous to interconnects 156 and 158 of bolometer 140 are indicated by 256 and 258. Similarly, the analogs of leads 170 and 174 are indicated by 270 and 274; note that in the preferred embodiment of FIG. 9d the leads are bifurcated.

In addition the dimensions, shapes, and materials of the stack forming the temperature dependent resistor may be varied, although the absorption efficiency depends upon the sheet resistance and processing-compatible materials are needed for manufacturability; the contact arrangement for the temperature dependent resistor could be varied such as one contact and one bottom contact so the electrode gap would not be needed, or two bottom contacts; the passivation layer (oxide 146 and 154 in preferred embodiment 140) on the temperature dependent resistor contacts could be omitted and thereby lower the thermal capacitance; the edges of the temperature dependent resistor could be passivated to limit surface leakage (such as

by oxide deposition after step (e) in the first preferred embodiment method); the air bridge interconnects 156 and 158 of bolometer 140 could be replaced by direct interconnect metal if the temperature dependent resistor is insulated to avoid the interconnects shorting out the top and bottom contacts; and the amorphous silicon resistive layer 150 could be heavily doped adjacent to the titanium nitride layers 148 and 152 in order to lower specific contact resistance and contact noise, of course the thickness of the high resistivity amorphous silicon will remain constant. See Column 10, line 61-67; and Column 11, line 1-6, and 19-44.

Hornbeck (663) still further discloses a method of fabrication of the bolometer and array is illustrated in FIGS. 8a-g and includes the following steps.

(a) Form load resistors 143, buffer amplifiers 120, capacitors 122, addressing circuitry, metal interconnections and protective oxide 190 in silicon substrate 142 by standard CMOS processing. Photolithographically form circular openings 194 of diameter two microns in oxide layer 190 for contacts from interconnects 156 and 158 down to bias voltage 182 and load resistors 143 and capacitors 122. Sputter on 3,000° thick aluminum 192 which fills the openings in oxide 190 as shown in dotted lines in FIG. 4b, and pattern and etch aluminum 192 to isolate interconnect contacts from ground plane; see FIG. 8a in which all of the circuitry below the oxide level 190 has been omitted for clarity.

(b) Spin on layer 196 of photoimageable polyimide to a thickness of 2.5 microns on aluminum layer 192, and expose and develop a pattern of circular openings 198 about two microns in diameter for interconnects 156 and 158. Next, bake to fully

imidize polyimide 196. See FIG. 8b in which the opening in oxide 190 has been suppressed for clarity. The interconnects 156 and 158 need not be located directly over openings 194, so the nonplanarity of aluminum 192 at openings 194 is not a problem.

(c) Sputter deposit in situ the layers that will form stack 144. In particular, place targets of oxide, titanium, and boron-doped silicon in a three target RF sputtering system. First sputter deposit a 500 ° thick oxide layer 154 from the oxide target in an argon atmosphere, next sputter deposit a 100 ° thick layer 152 of TiN from the titanium target in an argon/nitrogen atmosphere, then sputter deposit 500 ° thick layer 150 of boron-doped hydrogenated amorphous silicon from the boron-doped silicon target in an argon/hydrogen atmosphere, then another 100 ° thick TiN layer 148, and lastly another 500 ° thick oxide layer 146. See FIG. 8c, and note that polyimide 196 can withstand processing temperatures up to 300 degrees C, which may be required during the amorphous silicon deposition to insure a low density of gap states and correspondingly large conductivity activation energy.

(d) Spin on layer 200 of photoresist and expose and develop it to define stack 144 plus electrode gap 172 for each pixel. Plasma etch with the patterned photoresist 200 as etch mask in a plasma of $CF_4 + O_2$; this plasma etches oxide, TiN, and silicon and is stopped in the amorphous silicon layer by endpoint detection of SiF* species in the reaction products. See FIG. 8d.

(e) Strip photoresist 200 and spin on second layer 202 of photoresist and expose and develop it to define stack 144 without electrode gap 172. Plasma etch with the

patterned photoresist as etch mask in a plasma of CF_4 + O_2 to complete removal of the amorphous silicon, TiN, and oxide layers to form stack 144. This etch does not attack aluminum 192 and is stopped in polyimide 196 by endpoint detection of CO*; see FIG. 8e. Also, forming leads 170 and 174 from the same stack 144 as the temperature dependent resistor simplifies the processing.

(f) Strip second photoresist 202 and spin on third layer 204 of photoresist and expose and develop it to define the contacts 176 and 178. A wet etch of oxide 146 in a 10% solution of HF and with patterned photoresist 204 as etch mask, stops on TiN 148. The wet etch is isotropic and undercuts photoresist 204; see undercuts 206 in FIG. 8f. A light photoresist reflow sags photoresists 204 back to TiN 148 and eliminates the undercut overhang. Note that extreme selectivity in the etch is required because the TiN is only 100 ° thick, so is a sufficiently selective anisotropic plasma etch were used, then the undercut and consequent photoresist reflow would be avoided.

(g) Sputter deposit 5,000 ° layer 210 of Ti:W (an alloy of about 10% titanium to avoid the brittleness of pure tungsten) over patterned third photoresist 204. Spin on fourth layer 208 of photoresist and expose and develop it to define interconnects 156 and 158. Plasma etch the Ti:W in SF_6 with patterned fourth photoresist 208 as etch mask; this etch stops on photoresist 204. See FIG. 8g.

(h) Spin on PMMA (polymethylmethacrylate) for protection and saw the silicon wafers containing the bolometer arrays into chips. Spin and sprays the chips with chlorobenzene to remove the PMMA. Plasma ash the third and fourth photoresist

layers 204 and 208 together with the polyimide layer 196. This completes the chips except for bonding and packaging. Note that in FIG. 5a plasma etch access holes are shown in stack 144; these holes are etched through the oxide, TiN, and amorphous silicon layers when stack 144 is being formed and these holes reduces the amount of time required for the isotropic plasma ashing of the polyimide layer under stack 144. See Column 8, line 58-68; Column 9, line 1-68; and Column 10, Line 1-18.

Examiners Response to Arguments

4. Applicant's arguments filed 3-18-2004 have been fully considered but they are not persuasive.

Argument 1.

Applicant states that "The Office Action appears to confuse the following elements: the signal processing circuit (13) in the pending application, the silicon substrate (142) of Hornbeck, and the suspended layers constituting the active zones sensitive to radiation (10) of each detector, referred to also as bolometer (14) in Hornbeck. This confusion is resolved by reference to the fundamental characteristics of the present invention as defined in device Claim 17 and method-of-making-same Claim 22. The important fundamental characteristics include the microbridge-suspended layers of two neighboring detectors linked together by additional mechanical connections (15, 15'). These connections (15, 15') are separate from the mechanical support devices (11). This important feature is clearly shown at least in

Figures 8, 9 and 12 of the present pending application. The aforesaid recited features are distinctly different from Hornbeck and are not found in Hornbeck."

The applicant is respectfully directed to Hornbeck (663), Column 3, line 33-46, which states; FIGS. 4a-b are schematic cross sectional elevation views of bolometer 140 and FIG. 5a is a plan view; FIG. 5b illustrates in plan view a portion of array 106 showing the arrangement of the individual bolometers. Bolometer 140 includes a 1,700 ° thick and 50 microns square stack 144 made of a top 500° layer of silicon dioxide (oxide) 146, a 100 ° layer of titanium nitride (TiN) 148, a 500° layer of hydrogenated amorphous silicon (a-Si:H) 150 doped with boron to a carrier concentration of $2x10^{18}/cm^3$, another 100 ° layer of TiN 152, and a bottom 500 ° layer of silicon oxide 154. Stack 144 is supported over substrate 142 by two titanium tungsten (Ti:W) interconnects 156 and 158 located at diagonally opposite corners of the stack 144.

Also Column 3, line 57-68; and Column 4, line 1-12, which states; Vertical arrows 180 illustrate the direction of the direct current flow through a-Si:H 150. The current flow is from bias voltage supply 182 (5.8 volts) on substrate 142 through metal interconnect 156, into the half of TiN layer 148 on the contact 176 side of electrode gap 172, vertically down through a-Si:H 150 into TiN layer 152, vertically up through a-Si:H 150 into the half of TiN layer 148 on the contact 178 side of electrode gap 172, and lastly through interconnect 158 and load resistor 143 in substrate 142 to ground. The halves of TiN layer 148 and TiN layer 152 are highly conductive (about 800 $\mu\Omega$-cm resistivity) relative to a-Si:H 150 (about 1 MΩ-cm resistivity) and may be considered

equipotential surfaces. Thus resistor 141 is essentially two a-Si:H resistors in series, each a-Si:H resistor with a 500 A° length and a cross sectional shape of a 50 micron edge right triangle having a narrow notch extending from the right angle vertex nearly 90% of the way to the hypotenuse.

The examiner has interpreted from the Hornbeck (663) references above that stack 144 is supported over substrate 142 by interconnects 156 and 158, which are located at diagonally opposite corners of the stack 144. In addition, the stack 144 is separated into two sections by gap 172, which share the common resistor layer 141 of the stack 144. Thus the examiner has interpreted that bolometer 140 includes two microbridge detectors having their suspended layers linked together by the common resistor layer which is an additional mechanical connection separate from the supports.

The applicant is also respectfully directed to Figure 4a of Hornbeck (663), and Figure 11B of the applicants specification shown below, for purposes of comparison.

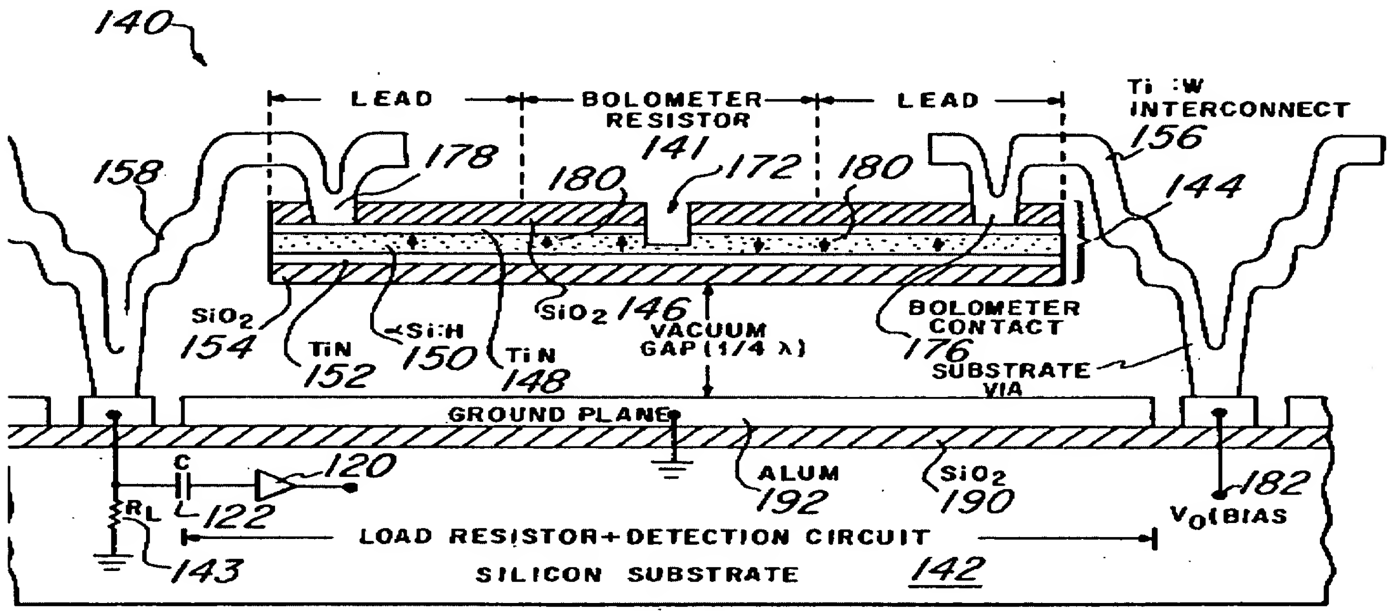

Fig.4a

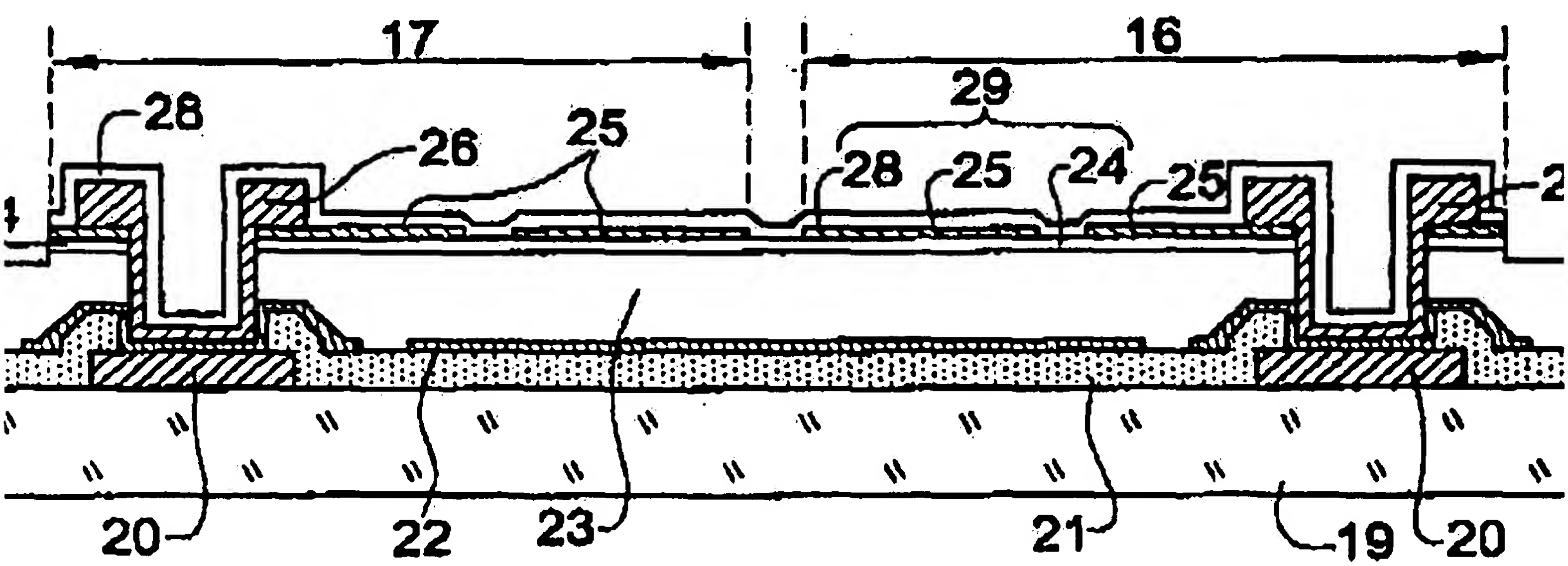

Fig. 11B

In addition, the applicant is directed to applicants specification page 11, lines 30, 31, and page 12, line 1-5, which state; There are at least 2 layers constituting the microbridge, which are later laid on the sacrificial layer 23:

- a layer 24 of heat-sensitive material which can be amorphous silicon laid following a classic process,

- a conducting coat 25 constituting the detector electrodes which can be titanium nitride laid by reactive sputtering.

The mechanical support and electrical interconnection devices whose realization will be described hereafter, are those of a microbridge in the field of infrared.

Also page 13, line 3-6, which states; A final photolithographical level facilitates definition of the detector perimeters by simultaneous etching of layers 24, 25 and 28 which results in;

- isolating the detectors from oné another',

- defining the heat insulation devices 12 cut in the microbridge 29 itself.

The examiner has interpreted from a comparison of Figure 4a and Figure 11B and the applicants specification referenced above, that stack 144 of Hornbeck (663) is equivalent to microbridge 29, and that both Figures above show two detectors linked together by an amorphous silicon layer with signal processing circuitry contained on their substrates.

Conclusion

5. The Amendment filed on 3-18-2004 under 37 CFR 1.131 has been considered but is ineffective to overcome the Lepejian (714) and Okubo (862) references.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications should be directed to Phillip Johnston whose telephone number is (571) 272-2475. The examiner can normally be reached on Monday-Friday from 7:30 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor John Lee can be reached at (571) 272-2477. The fax phone numbers are (703) 872-9318 for regular response activity, and (703) 872-9319 for after-final responses. In addition the customer service fax number is (703) 872- 9317.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

PJ
April 21, 2004

JOHN R. LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800